UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 7,584,441 B2
APPLICATION NO. : 10/665880
DATED : September 1, 2009
INVENTOR(S) : Alexander Gidon and David Knapp

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

On the title page, Item (57) the first line of the Abstract should be corrected as follows:

--A method for generating timing constraint systems, where the constrained object is a digital circuit[[.]], is provided, where the constraints are generated for the use of a digital logic optimization (syntheses) tool.--

Signed and Sealed this

Seventeenth Day of November, 2009

David J. Kappos

David J. Kappos
Director of the United States Patent and Trademark Office